Materials-Technology Co-Optimization (MTCO) for Inter-Die-Gap-Fill (IDGF) in Heterogeneous Integration of Chiplets

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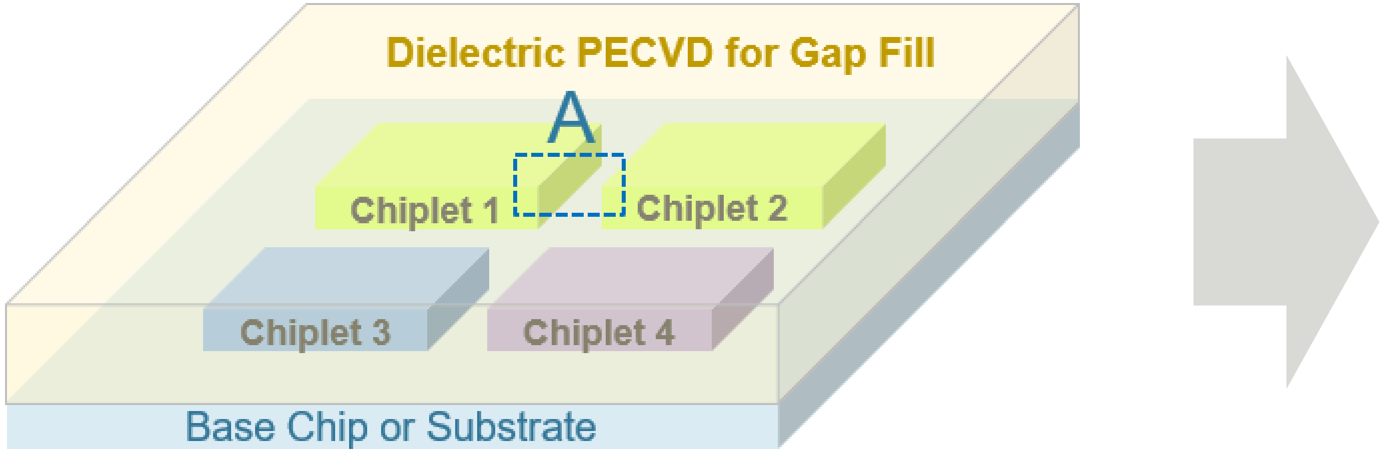
Outline

- Heterogeneous Integration
  - PECVD Inter-Die-Gap-Fill (IDGF)
  - Short Loop
- Failure Analysis
- PECVD Solutions
  - Materials Engineering: Interfaces, Mechanical, Thermal Properties
- Summary

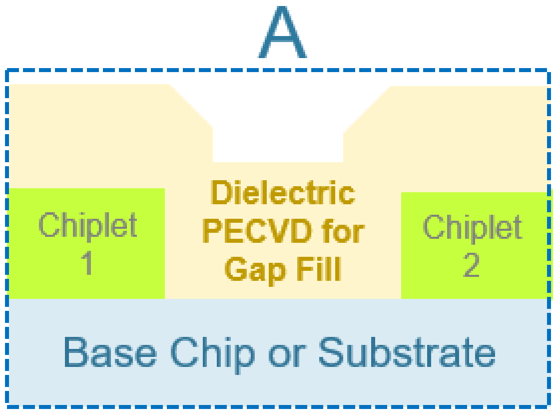
Heterogeneous Integration

High Performance Packaging:

Chiplet Hybrid Bonding ➔ PECVD Inter-Die-Gap-Fill (IDGF)



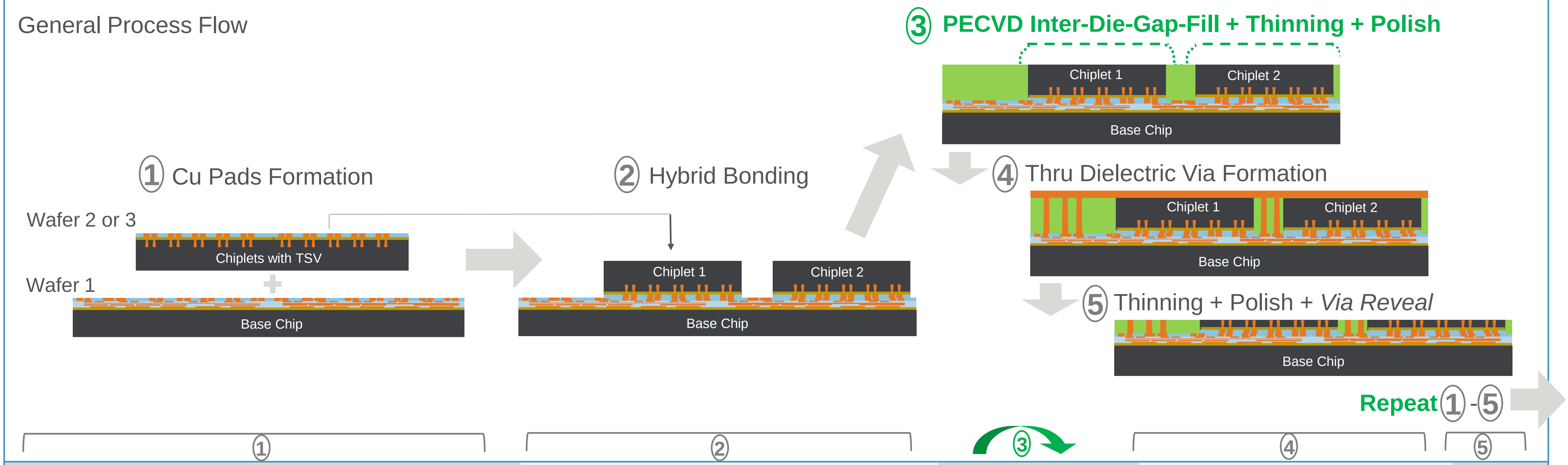
Cross-section at A



PECVD hardware, process, and new materials are tested for inter-die-gap-fill in heterogeneous integration

Applied Materials | Co-Optimization: Materials, Processes, Integration

Heterogeneous Integration of Chiplets



General Process Flow

① Cu Pads Formation

Wafer 2 or 3

Chiplets with TSV

Wafer 1

Base Chip

② Hybrid Bonding

Chiplet 1

Chiplet 2

Base Chip

③ PECVD Inter-Die-Gap-Fill + Thinning + Polish

Chiplet 1

Chiplet 2

Base Chip

④ Thru Dielectric Via Formation

Chiplet 1

Chiplet 2

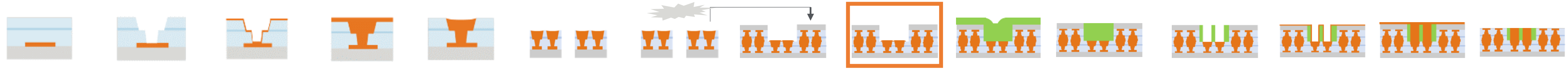
Base Chip

⑤ Thinning + Polish + *Via Reveal*

Base Chip

Repeat ① - ⑤

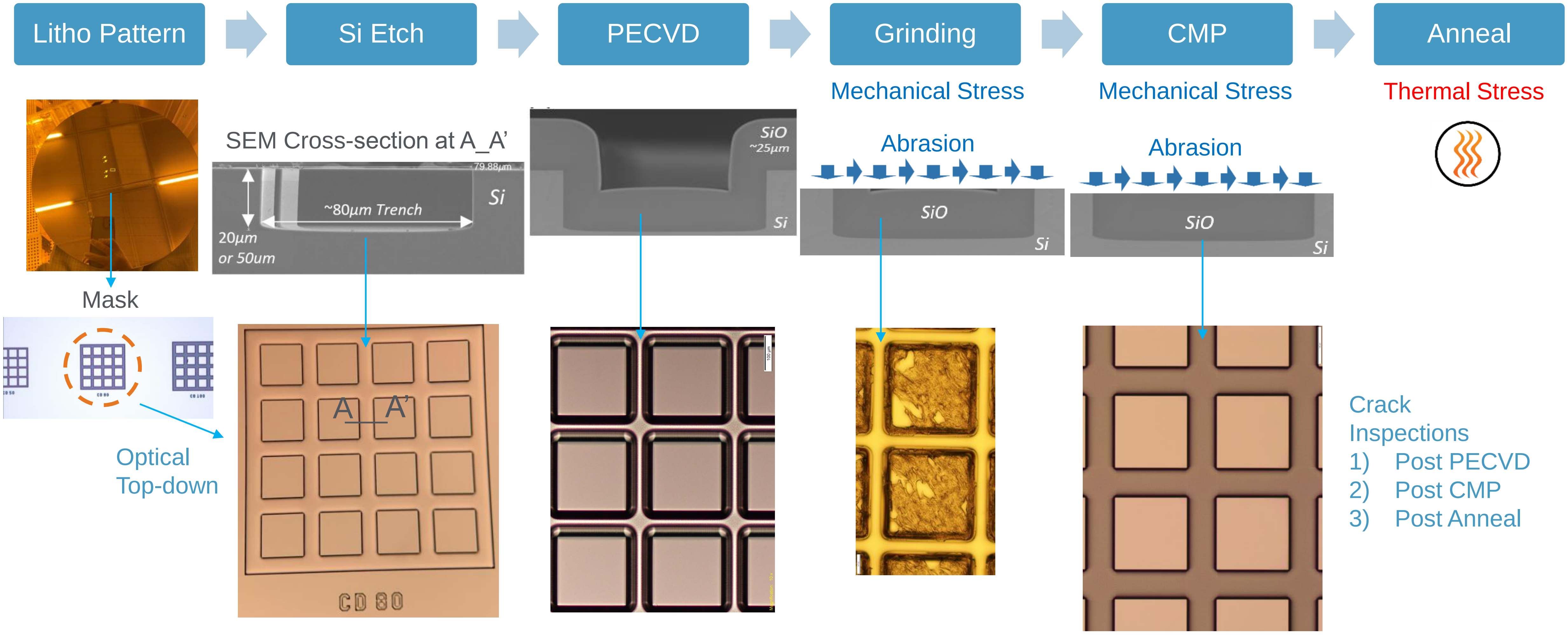
Unit Processes



①					②				③		④			⑤
ILD / Bonding Layers	Dual Damascene	Cu Barrier & Seed	Cu Fill	Polish	Wafer Singulation	Pre-Treatment	Hybrid Bonding	Bonding Anneal	Inter Die Gap Fill	Thinning Polish	Thru Dielectric Via	Cu Barrier & Seed	Cu Fill	Thinning Polish
Dielectric PECVD	Plasma Etch	PVD	ECD	CMP	Plasma Dicing	Plasma Wet Clean	Die Pick, Place, Bond	Furnace	Dielectric PECVD	Grinding CMP	Plasma Etch	PVD	ECD	CMP

Integration risks for PECVD Inter-Die-Gap-Fill: downstream mechanical and thermal processes

Applied Materials | Short Loop Proxy



Litho Pattern → Si Etch → PECVD → Grinding → CMP → Anneal

Grinding: Mechanical Stress

CMP: Mechanical Stress

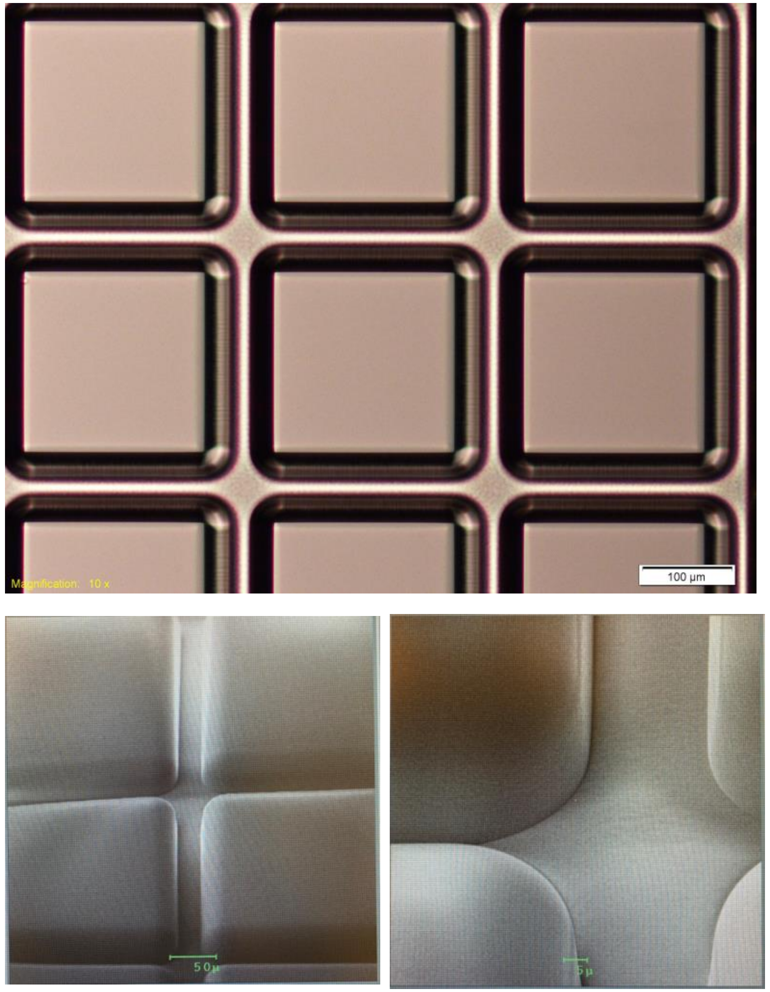
Anneal: Thermal Stress

Crack Inspections
1) Post PECVD
2) Post CMP
3) Post Anneal

Objective: test mechanical and thermal cracking stability of PECVD materials for heterogeneous integration

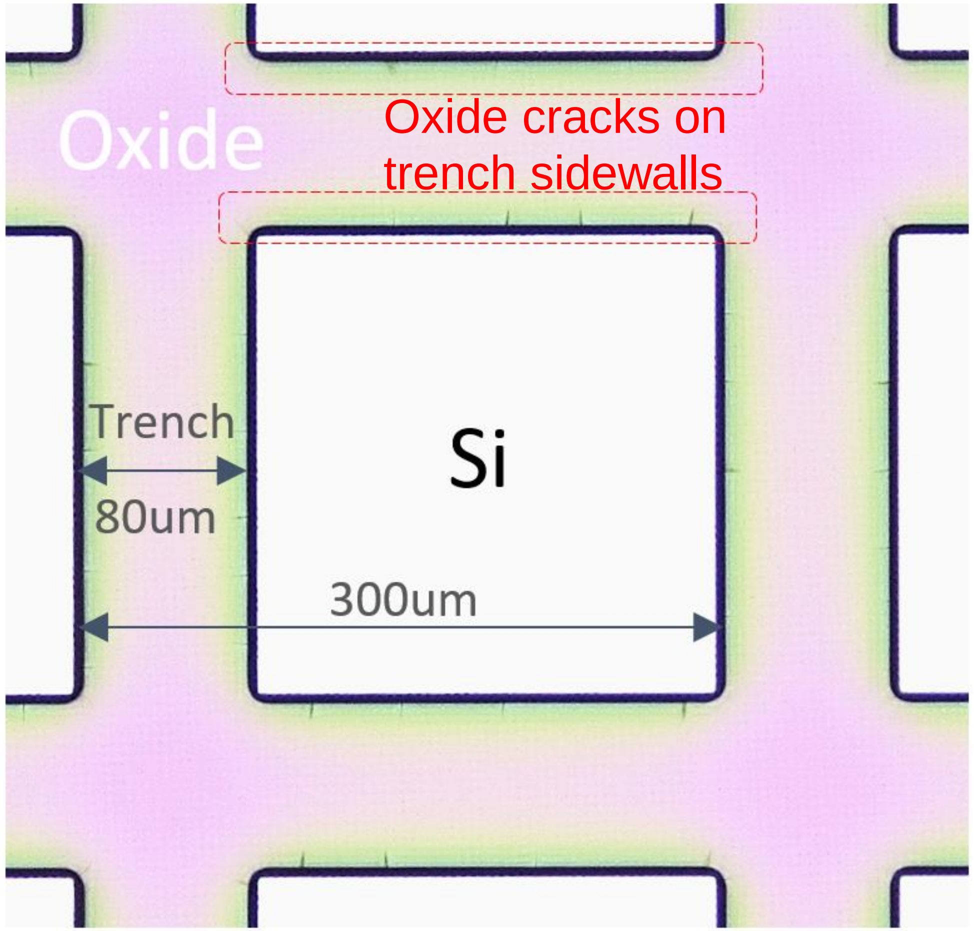
Optical Top-Down Crack Inspections

Post PECVD



No visible cracks after PECVD

Post CMP

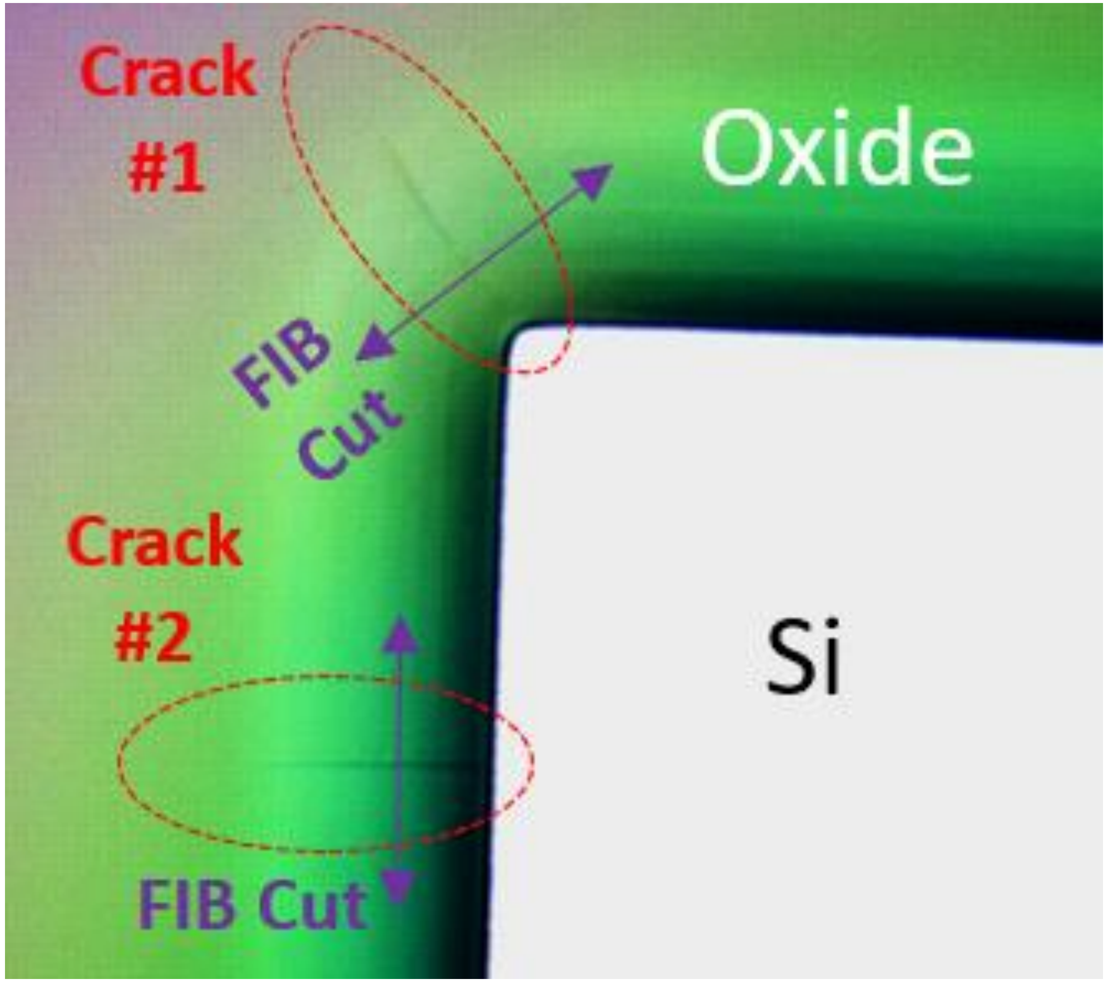


After Grinding + CMP, oxide hairline cracks on trench sidewalls with *unoptimized* PECVD

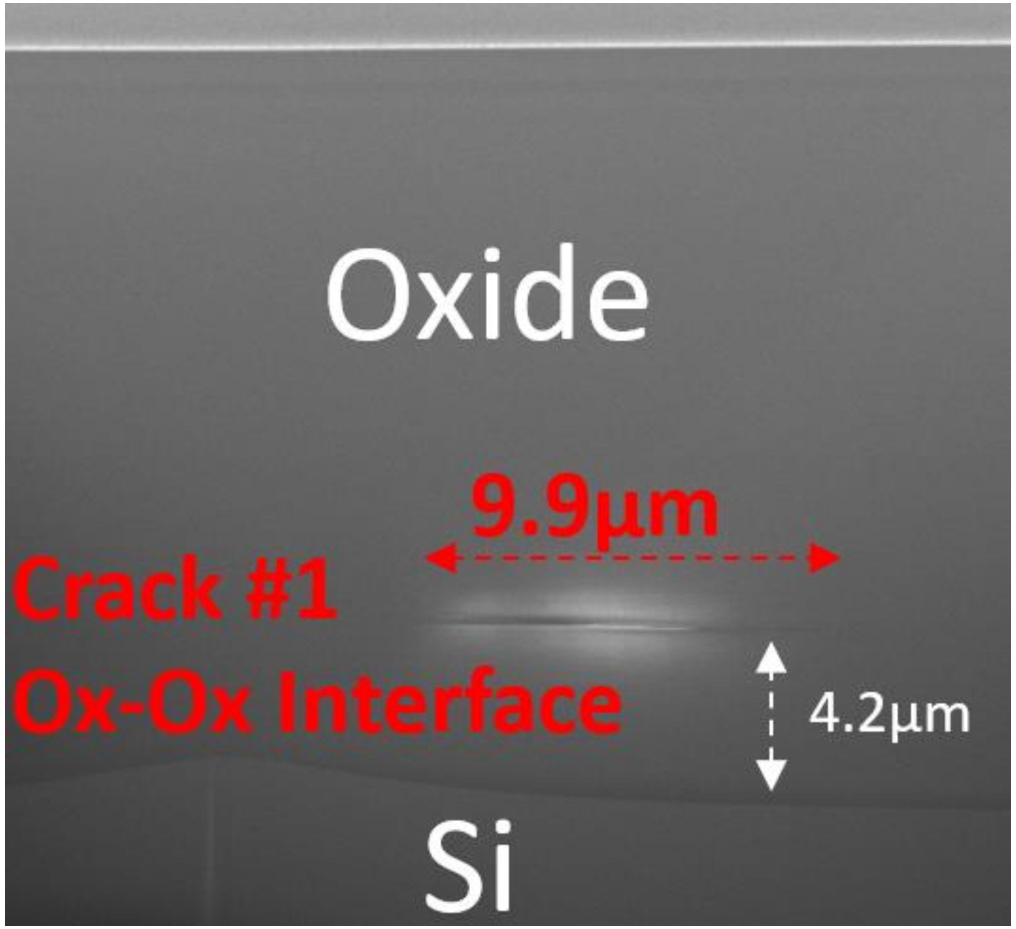
Next: failure analysis and PECVD solutions

Failure Analysis | Crack #1

Top-down optical zoom image of two oxide cracks

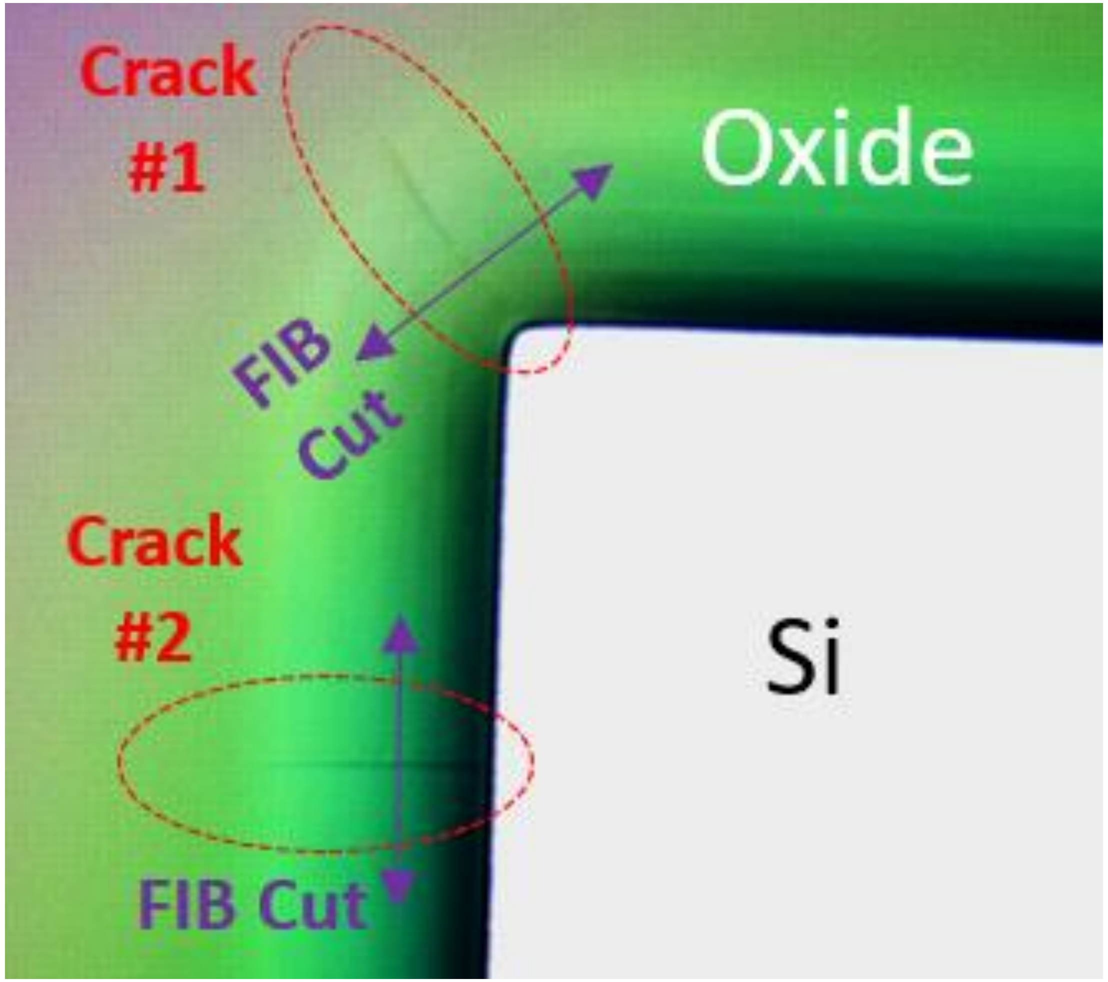


SEM cross-section show crack #1 is at the interface between oxide layers #1 and #2

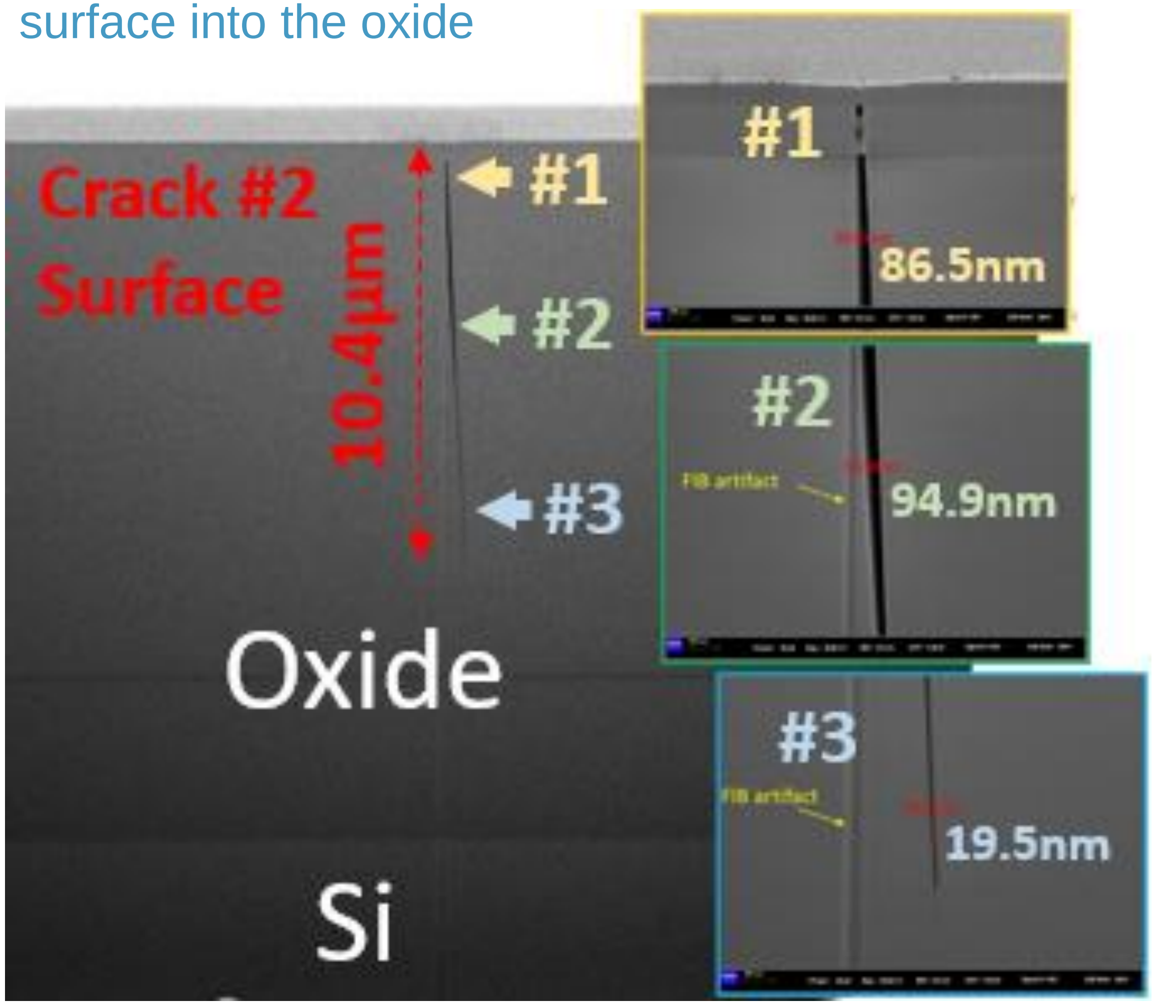


Failure Analysis | Crack #2

Top-down optical zoom image of two oxide cracks



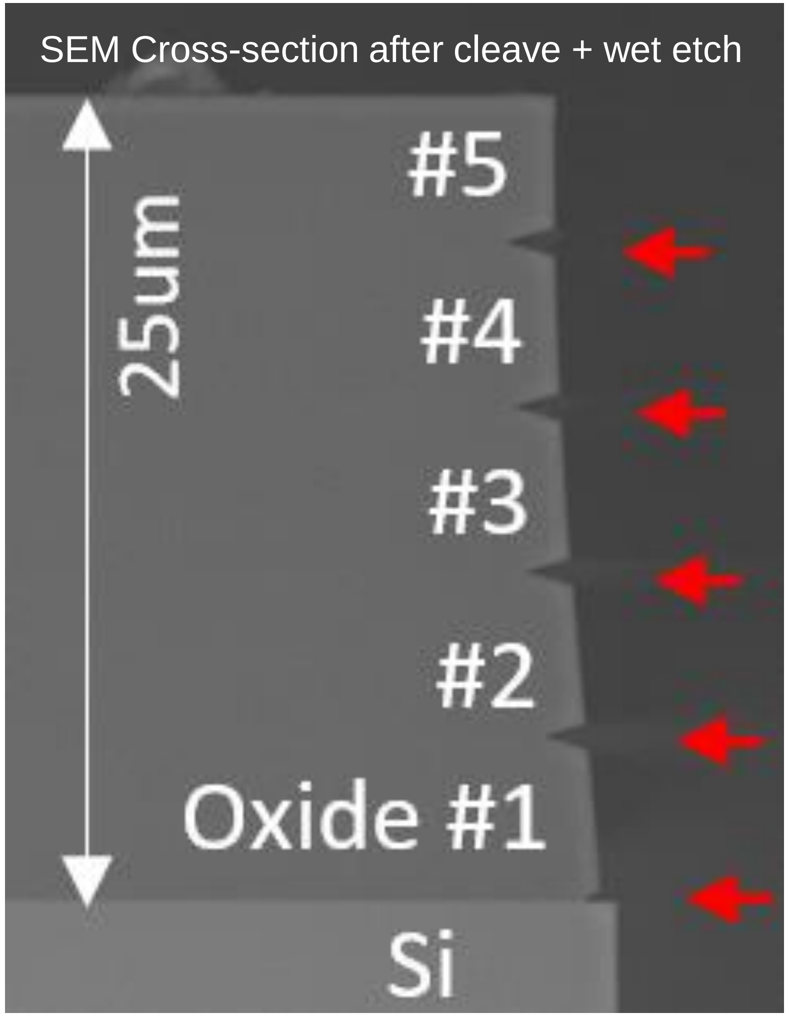
SEM cross-section show crack #2 extends from surface into the oxide



PECVD Materials Engineering | Interfaces vs. PECVD

Risk: interface flaws + stress (mechanical or thermal) ➔ crack initiation

Unoptimized PECVD


SEM Cross-section after cleave + wet etch

Optimized PECVD


SEM Cross-section after cleave + wet etch

PECVD hardware and recipe is optimized to eliminate interface flaws for homogeneous gap fill

PECVD Materials Engineering | Mechanical Cracks vs. PECVD

Risk: high modulus coatings + abrasive mechanical process ➔ crack initiation

PECVD Condition	**Post CMP** AMAT Si Trench TV (20um Deep x 80um Wide)
A	 ***~10 large oxide cracks on trench sidewall***
B	 ***5-10 oxide cracks | Smaller & Shorter***
C	 ***No visible cracks***

PECVD Oxide deposition is optimized to tune mechanical properties and eliminate cracks Post CMP

PECVD Materials Engineering | Mechanical Properties

Modulus & Hardness Measurements

Risk: high modulus coatings + abrasive mechanical process ➔ crack initiation

PECVD Condition	**Post CMP** AMAT Si Trench TV (20um Deep x 80um Wide)
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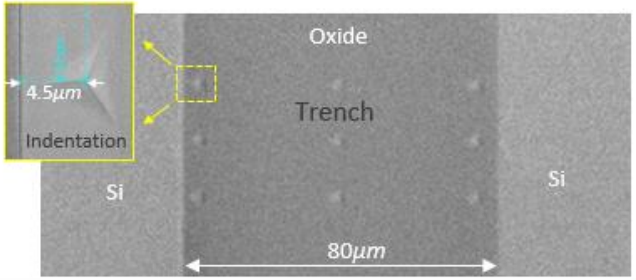
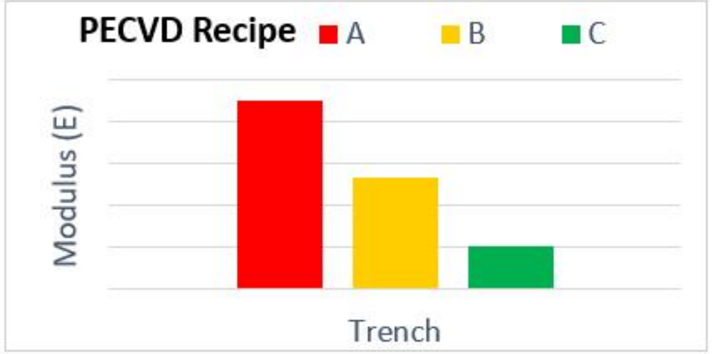
Scanning Probe Indentation





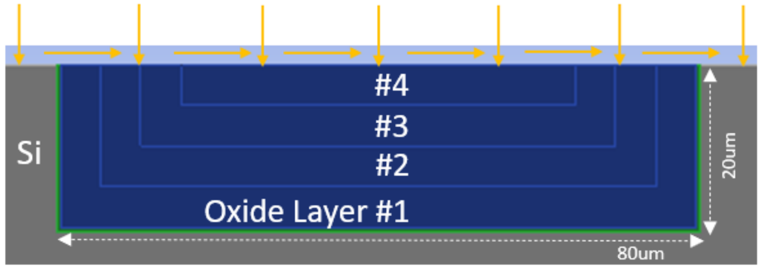
PECVD Oxide with lower modulus and hardness eliminates mechanical cracks Post CMP

PECVD Materials Engineering | Mechanical Stress Simulations

Risk: high modulus coatings + abrasive mechanical process ➔ crack initiation

Ansys Mechanical Finite Element Analysis (FEA) Software for Structural Engineering

Pressure load in vertical and lateral directions



Oxide Sidewall Modulus	Shear Stress Map in Oxide During Grinding Process
High E	 ★ High stress at oxide sidewall interfaces
Low E	 ★ Reduced stress

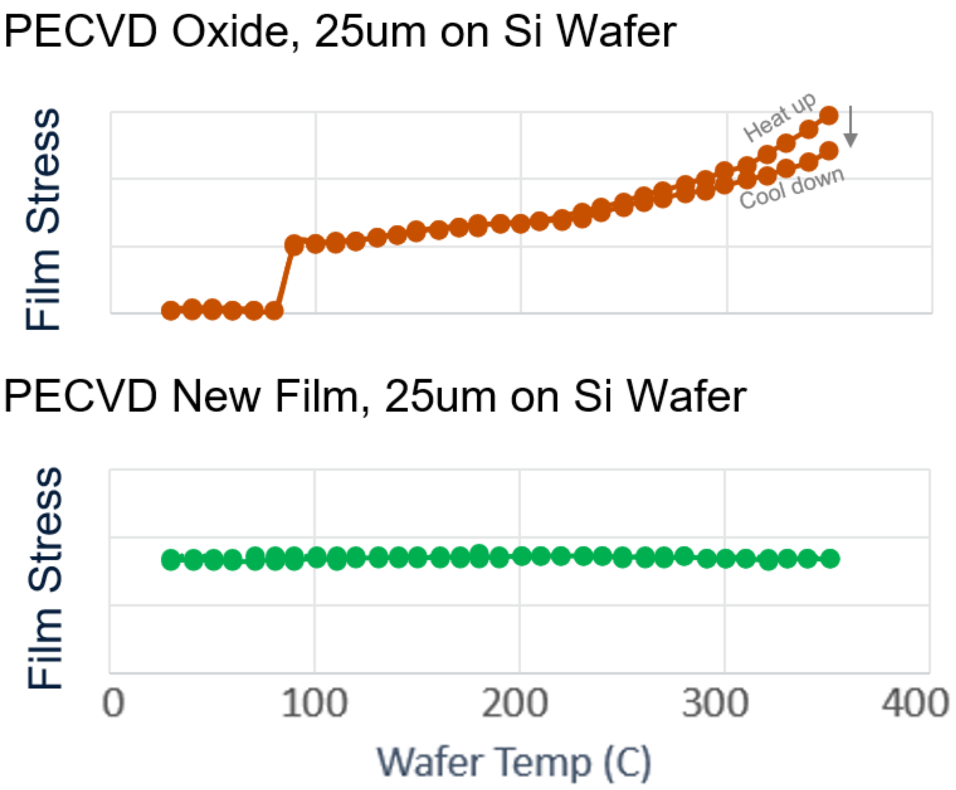
Simulation shows PECVD Oxide with lower modulus reduces shear stress during abrasive mechanical processes

PECVD Materials Engineering | Thermal Properties

CTE Measurements

Risk: material CTE differences ➔ thermal stress ➔ crack initiation

Wafer Thermal Deformation Measurements


PECVD Oxide, 25um on Si Wafer

PECVD New Film, 25um on Si Wafer

Coefficient of Thermal Expansion (CTE)

$$\frac{d\sigma_f}{dT} = -\frac{E_f}{1-\nu_f}(\alpha_f - \alpha_s)$$

σ_f = Film Stress

T = Temperature

α_f = Film CTE

E_f = Film Modulus

ν_f = Film Poisson Ratio, ~0.17

α_s = Silicon CTE, ~3.00ppm/C

J. Appl. Phys. 91, 1988–1992 (2002)

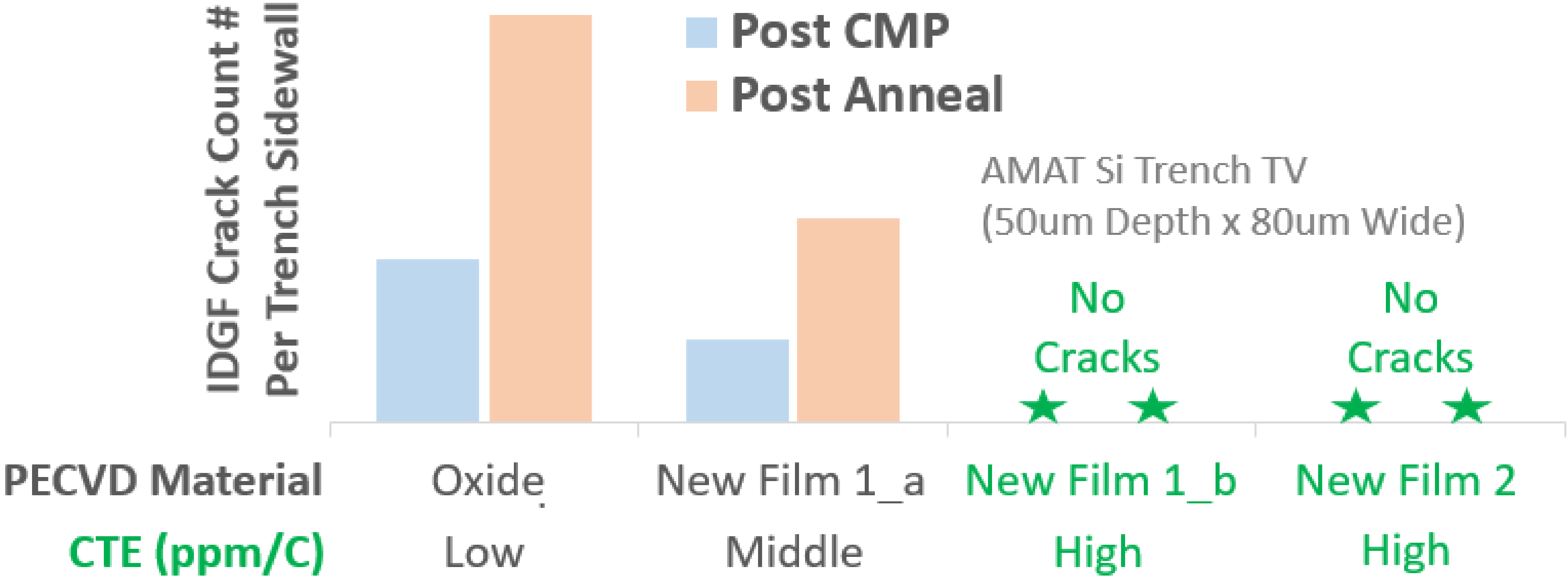
	$d\sigma_f / dT$ (MPa/C)	α_f = CTE (ppm/C)
PECVD Oxide	+ 0.1589	1.07
PECVD New Film	- 0.0015	3.02

$\alpha_{Silicon} \sim 3.00$ ★

CTE of PECVD New Film Material matches silicon ➔ low thermal stress

PECVD Materials Engineering | Thermal Cracks vs. PECVD

Risk: material CTE differences ➔ thermal stress ➔ crack initiation



PECVD New Film materials with CTE tuning eliminates thermal cracks Post Anneal

PECVD Materials Engineering | Thermal Stress Simulations

Risk: material CTE differences ➔ thermal stress ➔ crack initiation

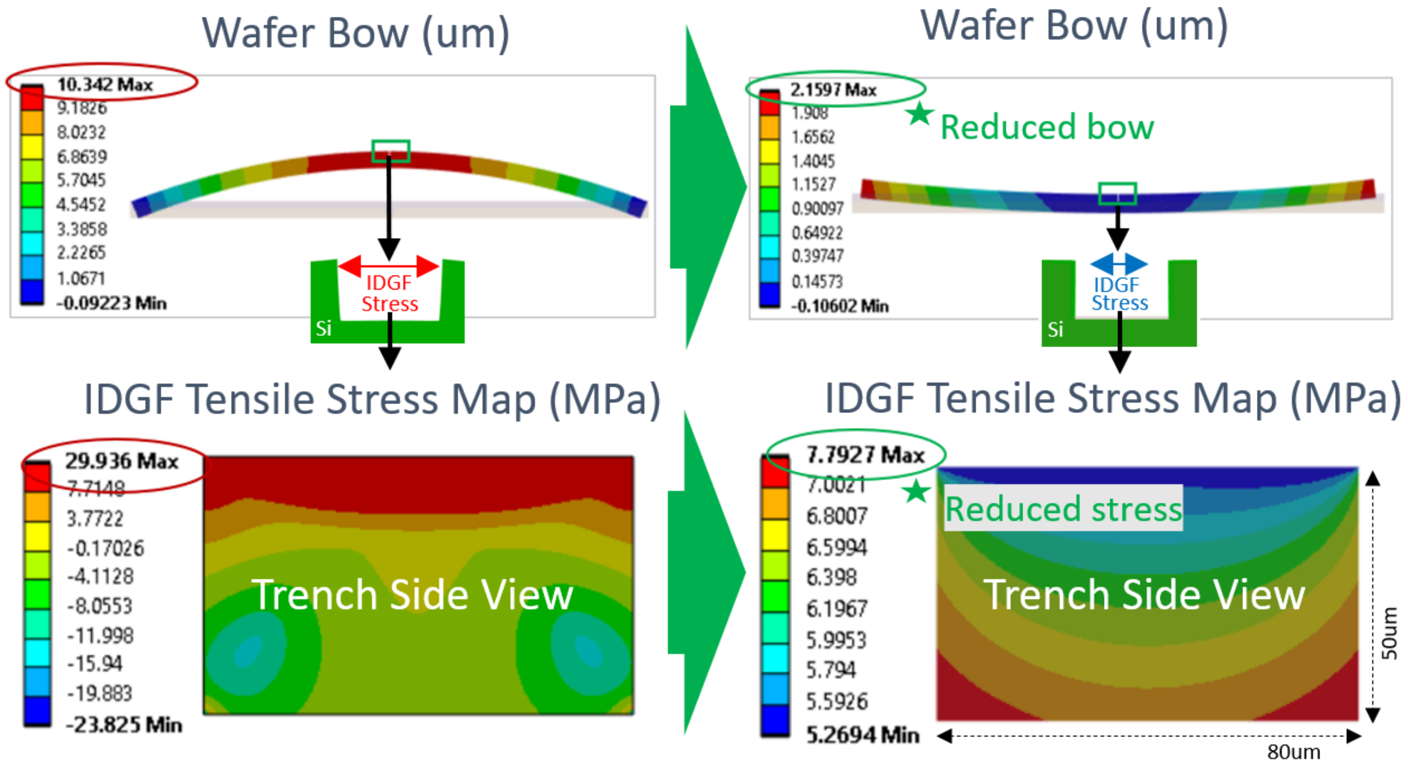
Ansys Mechanical Finite Element Analysis (FEA) Software for Structural Engineering

PECVD Oxide

CTE = 0.75 ppm/C

PECVD New Film

CTE = 3 ppm/C



Simulation shows PECVD New Film material with higher CTE reduces wafer bow and IDGF stress

Summary

- Demonstrated crack-free integration of Dielectric PECVD for Inter-Die-Gap-Fill (IDGF)

- Increasing resistance to integration cracks requires PECVD hardware, process, and **materials engineering**:
  - Eliminate interface flaws → for homogeneous gap fill
  - Lower modulus & hardness → to reduce film shear stress in mechanical Grinding & CMP
  - Higher CTE with new dielectric PECVD materials → to reduce film thermal stress in Anneal & Dep processes

- **Applied Materials enables integrated co-optimization** with equipment, process, and new materials for Heterogeneous Integration

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